IN THE CLAIMS

Please amend the claims to read as indicated herein.

1. (currently amended) A testing unit for testing a device under test (DUT), comprising:

a signal generator ~~adapted for applying~~ that applies a stimulus signal to the DUT,

a receiving unit ~~adapted for receiving~~ that receives a response signal from the DUT on the applied stimulus signal~~,~~; and

a synchronizing unit ~~for synchronizing~~ that synchronizes a data flow of the response signal between the DUT and the receiving unit~~, whereby~~;

wherein the synchronizing unit receives a first clock signal from the DUT and a second clock signal from the testing unit~~,~~; and

wherein the synchronizing unit ~~including~~ includes:

a buffer for buffering data~~,~~;

a write unit for writing data from the DUT into the buffer, ~~whereby~~ wherein the first clock signal controls a write access onto the buffer ~~is controlled by the first clock signal,~~; and

a read unit for reading out data from the buffer to be provided to the receiving unit, ~~whereby~~ wherein the second clock signal controls a read access onto the buffer ~~is controlled by the second clock signal~~.

2. (previously presented) The testing unit of claim 1, wherein the buffer comprises a register structure with a plurality of registers.

3. (currently amended) The testing unit of claim 2, further comprising:

a write pointer ~~adapted to be moved~~ that moves between the pluralities of registers for defining one of the plurality of registers to receive and buffer data from the DUT~~,~~; and

a read pointer ~~adapted to be moved~~ that moves between the plurality of registers for defining one of the pluralities of registers to be read out.

4. (currently amended) The testing unit of claim 3, wherein the write pointer is ~~adapted to be~~ clocked by the first clock signal for successively writing successive data words from the DUT to different registers, and the read pointer is ~~adapted to be~~ clocked by the second clock signal for successively reading out successive data words buffered in the plurality of registers.

5. (previously presented) The testing unit of claim 1, wherein the write unit comprises a latch controlled by the first clock signal, so that successive data words can be latched with the first clock signal and thus successively written into the buffer.

6. (currently amended) The testing unit of claim 1, wherein the buffer ~~is adapted to provide~~ provides an initial delay time between a first valid write access and a first valid read access.

7. (currently amended) The testing unit of claim 6, wherein the initial delay time is ~~provided~~ dependent on the maximum expected variation between such write and read accesses.

8. (currently amended) A method for testing a device under test (DUT), the method comprising:

applying a stimulus signal to the DUT, wherein the DUT outputs data in response to the stimulus signal;

writing ~~data in response to the stimulus signal from the DUT into a buffer, whereby a write access onto the buffer is controlled by a first clock signal of the DUT,~~ the data into a buffer, wherein the writing employs a first clock signal that controls a write access of the buffer, and wherein the first clock signal is provided by the DUT;

reading ~~out data from the buffer to be provided to a receiving unit, whereby a read access onto the buffer is controlled by a second clock signal of the receiving unit,~~ the data from the buffer, wherein the reading employs a second clock signal that controls a read access of the buffer, and wherein the second clock is provided by a receiving unit; and

~~receiving the read out data in response to the stimulus signal by~~ communicating the data from the buffer to the receiving unit.

9. (currently amended) The method of claim 8, further comprising initializing a first valid write access and/or a first valid read access.